REMARKS

This Amendment responds to the Office Action dated January 11, 2005 in which the Examiner rejected claim 4 under 35 U.S.C. §112 first paragraph, rejected claims 1-6 under 35 U.S.C. §112 second paragraph and under 35 U.S.C. §102(b).

Applicants respectfully traverse the Examiner's rejection of claim 4 under 35 U.S.C. §112 first paragraph. Applicants respectfully bring the Examiner's attention to page 12 lines 3-10 which provides support for claim 4. However, as an accommodation, claim 4 has been amended for stylistic reasons. The amendment is unrelated to a statutory requirement for patentability and does not narrow the literal scope of the claim.

As indicated above, claim 1 has been amended in order to more particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. Therefore, Applicants respectfully request the Examiner withdraws the rejection to claim 1-6 under 35 U.S.C. §112, second paragraph.

Claim 1 claims a semiconductor integrated circuit comprising a variable region and a fixed region. The variable region is to be subjected to a layout modification in conjunction with a change of a circuit component within the variable region. The fixed region is free from the layout modification in conjunction with the change of the circuit component within the variable region. The fixed region includes a circuit whose signal transfer characteristics are known in advance. Timing verification and evaluation of characteristics are carried out only on the variable region after layout modification.

Through the structure of the claimed invention a) having a fixed region which is free from layout modification and includes circuits whose signal transfer

characteristics are known in advance and b) timing verification and evaluation of characteristics are carried out only on the variable region after layout modification as claimed in claim 1, the claimed invention provides a semiconductor integrated circuit which reduces the time necessary for layout modification and characteristic verification and evaluation of the circuits involved in the modification. The prior art does not show, teach or suggest the invention as claimed in claim 1.

Claims 1-6 were rejected under 35 U.S.C. §102(b) as being anticipated by *Luk et al.* (U.S. Patent No. 5,883,814).

Luk et al. appears to disclose a method for system-on-chip layout automation which translates (compiles) a hardware description language (HDL) of a design, consisting of logic components and memory components, into a layout on a silicon chip, with optimized floor plan, macro and layout structures of logic and dynamic random access memory (DRAM) circuits. (col. 1, lines 8-14) FIG. 6 shows the different ways the DRAMs in the discrete case are integrated onto a single chip in the form of a number of DRAM macros. The on-chip DRAM macro configuration can be customized in terms of (1) the number M of on-chip DRAM macros, (2) the number Y of sub-DRAM macros in each DRAM macro, (3) the number X of basic DRAM building blocks (A) in each sub-DRAM macro, (4) the number B of I/O data-bits per macro, (5) the output driving power of the drivers in the DRAM macros to drive the external on-chip address, data, RAS, CAS, CE, etc., control buses as well as for the internal bit lines, word lines, and the like. The maximum number B_{max} of I/O for a DRAM macro is given by $B_{max} = X\ I_{max}$, where I_{max} is the maximum I/O the basic building block (A) can provide. (col. 4, lines 20-33) The methods described here integrate the logic macros and DRAM macros onto the same chips and optimizes for

their combined operations and overall performance, since the logic and DRAM components are accessible in the integration process. (col. 5, lines 29-33) The integrated system on a chip consists of a number of functionally distinct entities (or macros) as described earlier. Some of the entities such as microprocessor, graphic/video controller, digital signal processor have well defined, well specified internal basic cores which will not be modified at the time of design integration to form the more complex chip. (col. 6, lines 32-38) The parasitic, timing characteristic of the devices in the new layout have to be regenerated and the layout and logic/circuit database have to be updated. The timing analyzer 916 analyzes the timing of all the signals of the overall chip. It locates the slowest signals from chip inputs to latches, between latches, and from latch outputs to chip outputs. (col. 7, lines 55-61) The timing analyzer 916 analyzes the timing at the gate or transistor level, including the delay in the devices and the RC delay of the wiring to compute the overall signal delay, signal rise and fall time. The resistance, capacitance and RC delay information are stored in the RC timing database 921. They are obtained and computed from the extracted layout. The clock analyzer 916 does similar analysis for the clock signals. It analyzes the timing of the clock signals at all the latches, including clock wire delay and skew. The results of the timing analyzers are stored in the design database and are used as design parameters to optimize the logic and physical design at various stages. (col. 8, lines 1-13)

Thus, *Luke et al.* merely discloses a timing analyzer 916 which analyzes the timing of all signals of the overall chip. (col. 7, lines 58-61) Nothing in *Luk et al.* shows, teaches or suggests timing verification and evaluation of characteristics are carried out only on the variable region after layout modification as claimed in claim 1.

Rather, *Luk et al.* teaches away from the claimed invention since the timing analyzer 916 analyzes the timing of all signals of the overall chip (col. 7, lines 58-59).

Additionally, *Luk et al.* merely discloses some of the entities such as microprocessors, etc., have well-defined, well-specified internal basic cores which will not be modified at the time of the design integration to form the more complex chip (col. 6, lines 33-37). However, nothing in *Luk et al.* shows, teaches or suggests a fixed region that includes circuits who signal transfer characteristics are known in advance as claimed in claim 1. Rather, *Luk et al.* merely discloses that the circuits are well-defined and will not be modified (i.e. *Luk et al.* does not show, teach or suggest that the signal transfer characteristics are known in advance but only that the cores are well-defined and not modified). In fact, since column 7, lines 58-59 disclose that the timing analyzer 916 analysis the timing of all signals of the overall chip, *Luk et al.* teaches away from the claimed invention since the well-defined circuits are analyzed and thus their signal transfer characteristics are not know in advance.

Since nothing in *Luk et al.* shows, teaches or suggests a) a fixed region that includes circuits whose signal transfer characteristics are known in advance and b) timing verification and evaluation of characteristics are carried out only on the variable region after layout modification as claimed in claim 1, Applicants respectfully request the Examiner withdraws the rejection to claim 1 under 35 U.S.C. §102(b).

Claims 2-6 depend from claim 1 and recite additional features. Applicants respectfully submit that claims 2-6 would not have been anticipated by *Luk et al.* within the meaning of 35 U.S.C. §102(b) at least for the reasons as set forth above.

Therefore, Applicants respectfully request the Examiner withdraws the rejection to claims 2-6 under 35 U.S.C. §102(b).

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, the Examiner is requested to contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: April 1, 2005

By: _____
Ellen Marcie Emas
Registration No. 32,131

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620